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3	US 5617238 A	USPAT	19970401	21
4	US 5617237 A	USPAT	19970401	20
5	US 5612809 A	USPAT	19970318	20
6	US 5598360 A	USPAT	19970128	20
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8	US 5576877 A	USPAT	19961119	22
9	US 5569853 A	USPAT	19961029	9
10	US 5546325 A	USPAT	19960813	20
11	US 5455805 A	USPAT	19951003	9
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14	US 4009490 A	USPAT	19770222	13

1. Field of the Invention
The invention concerns synchronization of synchronous digital bit streams.

2. Description of the Prior Art

It is known to transmit information over a line in the form of a binary bit stream and processing of the information often entails reading the binary bit stream by means of the associated clock signal. This reading is generally effected by means of a D type flip-flop. The information is read on the rising or falling edge of the clock signal driving the flip-flop and passed to the output of the flip-flop. For the reading to be effected correctly the information has to be present for at least a setup time before the active (rising or falling) edge of the clock signal and for at least a hold time after this edge.

When there is more than one bit stream, each bit stream being transmitted by a respective line, the bit streams are made synchronous, in accordance with CCITT Recommendation G. 701, when their significant instants occur at exactly the same rate on average, the bit streams possibly being affected by amplitude jitter lying between specified limits.

It is therefore possible to read synchronous digital bit streams by means of a common clock signal running at the rate at which the significant instants of the bit streams occur, provided that the conditions in respect of setup and hold times are respected. As a general rule these conditions do not raise any problem when the information is at a low bit rate. On the other hand, it becomes necessary to synchronize the bit streams when the hold and setup times and the spread in propagation time in the logic circuits and amplifiers sending the bit streams and in the transmission lines are no longer negligible in comparison with the bit duration, in other words when the bit streams have a high bit rate.

An object of the invention is to synchronize synchronous digital bit streams, in particular to enable them to be read by a common clock signal.

SUMMARY OF THE INVENTION

In one aspect, the invention consists in a method of synchronizing synchronous digital bit streams each comprising bits each having the same bit duration, wherein one of said bit streams is taken as a reference and provides a basis for defining successive reference time intervals each equal to said bit duration, a plurality of timing windows are defined within each reference time interval, a second bit stream is subjected to a time delay that may have a null or zero value, one of said windows is taken as a reference window on the basis of a required phase relationship between said reference bit stream and said second bit stream, the phases of said reference bit stream and said second bit stream are compared and the second bit stream is read when the phase of said second bit stream is within the reference window.

ing said reference digital bit stream, a phase comparator connected to said timing window generator, a time delay selector connected to said phase comparator.

10 connected to said timing window generator, a time delay selector connected to said phase comparator, a plurality of time-delay circuits each imposing a respective time delay which is a multiple of a common basic time-delay, adapted to be connected to a second line carrying a second digital bit stream before it is subjected to a time-delay, a plurality of inputs of said switching device adapted to be connected to said second line and to a time-delay circuit, a plurality of outputs of said switching device being one greater than the number of time-delay circuits, an output of said switching device adapted to be connected to a third line carrying a second digital bit stream after it is subjected to said time-delay circuit and an input of said phase comparator adapted to be connected to said third line.

15 The method in accordance with the invention requires that the synchronous digital bit streams comprise a minimum number of transitions, a condition which is generally met when they are from an optical or coaxial line terminal comprising a limited sum encoder/scrambler.

Other objects and advantages will appear from following description of examples of the invention when considered in connection with the accompanying drawings, and the novel features will be particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of a device in accordance with the invention for synchronizing two bit streams.

FIG. 2 is a diagram showing timing windows as defined by a circuit from FIG. 1.

FIG. 3 shows one example of the method of synchronizing two digital bit streams.

FIG. 4 shows another example of the method of synchronizing two digital bit streams.

FIG. 5 represents a state diagram relating to FIG. 1.

FIG. 6 represents a state diagram relating to FIG. 2.

FIG. 7 shows one embodiment of the device in accordance with the invention.

FIG. 8 shows another embodiment of the device in accordance with the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the device shown in block diagram form in FIG. 1, two lines 1 and 2 carry respective synchronous digital bit streams A and B each with the same bit duration. The time-delay devices L1R1 through L3R3 have their inputs connected to line 1 and their output connected to switching device 3; line 2 is also connected directly to switching device 3.

